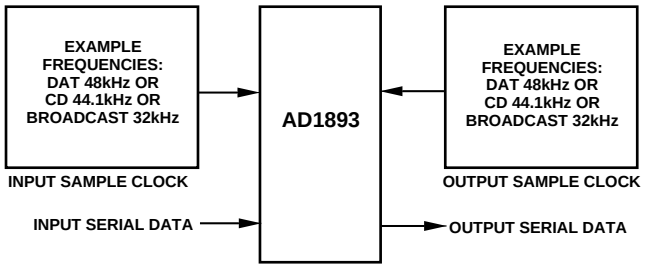
# Low Cost SamplePort® 16-Bit Stereo Asynchronous Sample Rate Converter

# AD1893

**FEATURES**
**Low Cost**
**LQFP and PDIP Packages**
**3 V Supply Performance Specified—Very Low Power**
**Automatically Senses Sample Frequencies—No Programming Required**
**Rejects Sample Clock Jitter**
**Accommodates Dynamically Changing Asynchronous Sample Clocks**
**8 kHz to 56 kHz Sample Clock Frequency Range**
**Approximately 1:2 to 2:1 Ratio Between Sample Clocks**
**–96 dB THD+N at 1 kHz**
**96 dB Dynamic Range**
**Optimal Clock Tracking Control—Slow/Fast Settling Modes**
**Linear Phase in All Modes**
**Automatic Output Mute**
**Flexible Four-Wire Serial Interfaces with Right-Justified Mode**
**Power-Down Mode**
**On-Chip Oscillator**

**APPLICATIONS**
**Consumer CD-R, DAT, DCC, MD and 8 mm Video Tape Recorders Including Portables**
**Digital Audio Communication/Network Systems**
**Computer Multimedia Systems**

**SYSTEM DIAGRAM**


EXAMPLE FREQUENCIES: DAT 48kHz OR CD 44.1kHz OR BROADCAST 32kHz
AD1893
EXAMPLE FREQUENCIES: DAT 48kHz OR CD 44.1kHz OR BROADCAST 32kHz
INPUT SAMPLE CLOCK
OUTPUT SAMPLE CLOCK
INPUT SERIAL DATA
OUTPUT SERIAL DATA

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## PRODUCT OVERVIEW

The AD1893 SamplePort is a fully digital, stereo Asynchronous Sample Rate Converter (ASRC) that solves sample rate interfacing and compatibility problems in digital audio equipment. Conceptually, this converter interpolates the input data up to a very high internal sample rate with a time resolution of 300 ps, then decimates down to the desired output sample rate. The AD1893 is intended for 16-bit low cost, non-varispeed applications where low voltage, low power (i.e., battery-powered) operation is required. Refer to the AD1890/AD1891 data sheet for other products in the SamplePort family. This device is asynchronous because the frequency and phase relationships between the input and output sample clocks (both are inputs to the AD1893 ASRC) are arbitrary and need not be related by a simple integer ratio. There is no need to explicitly select or program the input and output sample clock frequencies, as the AD1893 automatically senses the relationship between the two clocks. The input and output sample clock frequencies can nominally range from 8 kHz to 56 kHz, and the ratio between them can vary from approximately 1:2 to 2:1.

SamplePort is a registered trademark of Analog Devices, Inc.

The AD1893 uses multirate digital signal processing techniques to construct an output sample stream from the input sample stream. The input word width is 4 to 16 bits for the AD1893. Shorter input words are automatically zero-filled in the LSBs. The output word width is 24 bits. The user can receive as many of the output bits as desired. Internal arithmetic is performed with 22-bit coefficients and 27-bit accumulation. The digital samples are processed with unity gain.

The input and output control signals allow for considerable flexibility for interfacing to a variety of DSP chips, AES/EBU receivers and transmitters and for I²S compatible devices. Input and output data can be independently right- or left- (with or without a one bit clock delay) justified to the left/right clock edge. In the right-justified mode, the MSB is delayed 16-bit clock periods from the left/right clock edge transition. Input and output data can also be independently justified to the word clock rising edge. The data justification options are encoded on two mode pins for both the input port and the output port. The bit clocks can also be independently configured for rising edge active or falling edge active operation.

The AD1893 SamplePort ASRC has on-chip digital coefficients that correspond to a highly oversampled 0 Hz to 20 kHz low-pass filter with a flat passband, a very narrow transition band, and a high degree of stopband attenuation. A subset of these filter coefficients are dynamically chosen on the basis of the filtered ratio between the input sample clock ($L\overline{R}\_I$) and the output sample clock ($L\overline{R}\_O$), and these coefficients are then used in an FIR convolver to perform the sample rate conversion. Refer to the Theory of Operation section of this data sheet for a more thorough functional description. The low-pass filter has been designed so that full 20 kHz bandwidth is maintained when the input and output sample clock frequencies are as low as 44.1 kHz. If the output sample rate drops below the input sample rate, the bandwidth of the input signal is automatically

*(continued on Page 4)*

REV. A

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**One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.**
**Tel: 781/329-4700 World Wide Web Site: http://www.analog.com**
**Fax: 781/326-8703**
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# AD1893–SPECIFICATIONS

**TEST CONDITIONS UNLESS OTHERWISE NOTED**

| | | |
|---|---|---|
| Supply Voltage | +3.0 | V |
| Ambient Temperature | 25 | °C |
| Crystal Frequency | 16 | MHz |
| Load Capacitance | 100 | pF |

All minimums and maximums tested except as noted.

**PERFORMANCE**[1] (Guaranteed for $V_{DD}$ = +3.3 V to +5.0 V ± 10%)

| | Min | Max | Units |
|---|---|---|---|
| Dynamic Range (20 Hz to 20 kHz, –60 dB Input) | 96 | | dB |
| Total Harmonic Distortion + Noise | | | |
| (20 Hz to 20 kHz, Full-Scale Input, $F_{SOUT}/F_{SIN}$ Between 0.51 and 1.99) | | –94 | dB |
| (1 kHz Full-Scale Input, $F_{SOUT}/F_{SIN}$ Between 0.7 and 1.4) | | –96 | dB |
| (10 kHz Full-Scale Input, $F_{SOUT}/F_{SIN}$ Between 0.7 and 1.4) | | –95 | dB |
| Interchannel Phase Deviation | | 0 | Degrees |
| Input and Output Sample Clock Jitter | | | |
| (For ≤1 dB Degradation in THD+N with 10 kHz Full-Scale Input, Slow-Settling Mode) | 10 | | ns |

**DIGITAL INPUTS** (Guaranteed for $V_{DD}$ = +3.0 V to +5.0 V ± 10%)

| | Min | Max | Units |
|---|---|---|---|
| $V_{IH}$ | 2.0 | | V |
| $V_{IL}$ ($V_{DD} \geq$ +3.0 V) | | 0.8 | V |
| $V_{IL}$ (+2.7 V ≤ $V_{DD}$ < +3.0 V) | | 0.7 | V |
| $I_{IH}$ @ $V_{IH}$ = +5.0 V, All Pins Except XTAL_I | | 4 | µA |
| $I_{IH}$ @ $V_{IH}$ = +5.0 V, XTAL_I Pin | | 6 | µA |
| $I_{IL}$ @ $V_{IL}$ = 0 V, All Pins Except XTAL_I | | 4 | µA |
| $I_{IL}$ @ $V_{IL}$ = 0 V, XTAL_I Pin | | 6 | µA |
| $V_{OH}$ @ $I_{OH}$ = –4 mA ($V_{DD} \geq$ +3.0 V) | 2.4 | | V |
| $V_{OH}$ @ $I_{OH}$ = –4 mA (+2.7 V ≤ $V_{DD}$ < +3.0 V) | 2.2 | | V |
| $V_{OL}$ @ $I_{OL}$ = 4 mA | | 0.4 | V |
| Input Capacitance[1] | | 15 | pF |

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**DIGITAL TIMING** (Guaranteed for $V_{DD}$ = +3.0 V to +5.0 V ± 10%) See Figures 26 through 28.

| | | Min | Max | Units |
|---|---|---|---|---|
| $t_{CRYSTAL}$ | Crystal Period | 62.5 | 125 | ns |
| $F_{CRYSTAL}$ | Crystal Frequency ($1/t_{CRYSTAL}$) | | 16 | MHz |
| $t_{PWL}$ | Crystal LO Pulsewidth | 20 | | ns |
| $t_{PWH}$ | Crystal HI Pulsewidth | 20 | | ns |
| $F_{LRI}$ | $\overline{LR}$_I Frequency with 16 MHz Crystal[1] | 10 | 56 | kHz |
| $t_{RPWL}$ | $\overline{RESET}$ LO Pulsewidth | 125 | | ns |
| $t_{RS}$ | $\overline{RESET}$ Setup to Crystal Falling | 15 | | ns |
| $t_{BCLK}$ | BCLK_I/O Period[1] | 120 | | ns |
| $F_{BCLK}$ | BCLK_I/O Frequency ($1/t_{BCLK}$)[1] | | 8.33 | MHz |
| $t_{BPWL}$ | BCLK_I/O LO Pulsewidth | 55 | | ns |
| $t_{BPWH}$ | BCLK_I/O HI Pulsewidth | 55 | | ns |
| $t_{WSI}$ | WCLK_I Setup to BCLK_I | 15 | | ns |
| $t_{WSO}$ | WCLK_O Setup to BCLK_O | 40 | | ns |
| $t_{LRSI}$ | $\overline{LR}$_I Setup to BCLK_I | 15 | | ns |
| $t_{LRSO}$ | $\overline{LR}$_O Setup to BCLK_O | 55 | | ns |
| $t_{DS}$ | Data Setup to BCLK_I | 0 | | ns |
| $t_{DH}$ | Data Hold from BCLK_I | 35 | | ns |
| $t_{DPD}$ | Data Propagation Delay from BCLK_O | | 90 | ns |
| $t_{DOH}$ | Data Output Hold from BCLK_O | 15 | | ns |

**DIGITAL FILTER CHARACTERISTICS**[1]

| | Min | Max | Units |
|---|---|---|---|
| Passband Ripple (0 kHz to 20 kHz) | | 0.01 | dB |
| Transition Band[2] | | 4.1 | kHz |
| Stopband Attenuation | 110 | | dB |
| Group Delay ($L\overline{R}\_I$ = 50 kHz) | 700 | 3000 | µs |

**POWER** ($F_{SIN}$ = 48 kHz, $F_{SOUT}$ = 44.1 kHz)

| | Min | Typ | Max | Units |
|---|---|---|---|---|
| Supplies | | | | |
| Voltage, $V_{DD}$ | 2.7 | | 5.5 | V |
| Operational Current, $I_{DD}$ ($V_{DD}$ = +5.0 V) | | 30 | 40 | mA |
| Operational Current, $I_{DD}$ ($V_{DD}$ = +3.0 V)[1] | | 15 | 20 | mA |
| Power-Down Current, $I_{DD}$ ($V_{DD}$ = +5.0 V) | | 1.5 | 2.5 | mA |
| Power-Down Current, $I_{DD}$ ($V_{DD}$ = +3.0 V)[1] | | 0.5 | 1.0 | mA |
| Dissipation[1] | | | | |
| Operation ($V_{DD}$ = +5.0 V) | | 150 | 200 | mW |
| Operation ($V_{DD}$ = +3.0 V) | | 45 | 60 | mW |
| Power-Down ($V_{DD}$ = +5.0 V) | | 7.5 | 12.5 | mW |
| Power-Down ($V_{DD}$ = +3.0 V) | | 1.5 | 3.0 | mW |

**TEMPERATURE RANGE**

| | Min | Max | Units |
|---|---|---|---|
| Specifications Guaranteed | 0 | +70 | °C |
| Operational Guaranteed | –40 | +85 | °C |
| Storage | –60 | +100 | °C |

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**ABSOLUTE MAXIMUM RATINGS**[3]

| | Min | Max | Units |
|---|---|---|---|
| $V_{DD}$ to GND | –0.3 | 7.0 | V |
| DC Input Voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| Latch-Up Trigger Current | –1000 | +1000 | mA |
| Soldering | | +300 | °C |
| | | 10 | sec |

NOTES

[1]Guaranteed, Not Tested

[2]Valid only when $F_{SOUT} \geq F_{SIN}$ (i.e., upsampling), $F_{SIN}$ = 44.1 kHz.

[3]Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Specifications subject to change without notice.

**ORDERING GUIDE**

| Model | Temperature Range | Package Descriptions | Package Options |
|---|---|---|---|
| AD1893JN | 0°C to +70°C | Plastic DIP | N-28 |
| AD1893JST | 0°C to +70°C | LQFP | ST-44 |

**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1893 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

*(continued from Page 1)*

**PRODUCT OVERVIEW (Continued)**

limited to avoid alias distortion on the output signal. The AD1893 dynamically alters the low-pass filter cutoff frequency smoothly and slowly, so that real-time variations in the sample rate ratio are possible without degradation of the audio quality.

The AD1893 has a pin selectable slow- or fast-settling mode. This mode determines how quickly the ASRC adapts to a change in either the input sample clock frequency ($F_{SIN}$) or the output sample clock frequency ($F_{SOUT}$). In the slow-settling mode, the control loop which computes the ratio between $F_{SIN}$ and $F_{SOUT}$ settles in approximately 800 ms and begins to reject jitter above 3 Hz. The slow-settling mode offers the best signal quality and the greatest jitter rejection. In the fast-settling mode, the control loop settles in approximately 200 ms and begins to reject jitter above 12 Hz. The fast-settling mode allows rapid, real time sample rate changes to be tracked without error, at the expense of some narrowband noise modulation products on the output signal.

The AD1893 features short group delay processing. This feature relates to the depth of the First-In, First-Out (FIFO) memory, which buffers the input data samples before they are processed by the FIR convolver. In the AD1893, the group delay is approximately 700 µs. If the read and write pointers that manage the FIFO cross (indicating underflow or overflow), the AD1893 asserts the mute output (MUTE_O) pin HI for 128 output clock cycles. If MUTE_O is connected to the mute input (MUTE_I) pin, as it normally should be, the serial output will be muted (i.e., all bits zero) during this transient event.

The AD1893 includes an on-chip oscillator that only requires the user provide an external crystal. By removing the need for an external oscillator, the AD1893 lowers the total cost of ownership to the end user. The AD1893 also includes a power-down mode, which is invoked with the PWRDWN pin. Asserting this control signal HI will place the AD1893 into a very low power dissipation in active and standby condition.

The AD1893 is fabricated in a 0.8 µm single poly, double metal CMOS process and are packaged in a 0.6" wide 28-lead plastic DIP and a 10 mm by 10 mm body size 44-lead LQFP. The AD1893 operates from a +3 V to +5 V power supply over the temperature range of 0°C to +70°C.

**DEFINITIONS**

**Dynamic Range**

The ratio of a near full-scale input signal to the integrated noise in the passband (0 kHz to ≈20 kHz), expressed in decibels (dB). Dynamic range is measured with a –60 dB input signal and "60 dB" arithmetically added to the result.

**Total Harmonic Distortion + Noise**

Total Harmonic Distortion plus Noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the values of the harmonics and noise to the rms value of a sinusoidal input signal. It is usually expressed in percent (%) or decibels.

**Interchannel Phase Deviation**

Difference in input sampling times between stereo channels, expressed as a phase difference in degrees between 1 kHz inputs.

**Group Delay**

Intuitively, the time interval required for a full-level input pulse to appear at the converter's output, at full level, expressed in milliseconds (ms). More precisely, the derivative of radian phase with respect to radian frequency at a given frequency.

**Transport Delay**

The time interval between when an impulse is applied to the converter's input and when the output starts to be affected by this impulse, expressed in milliseconds (ms). Transport delay is independent of frequency.

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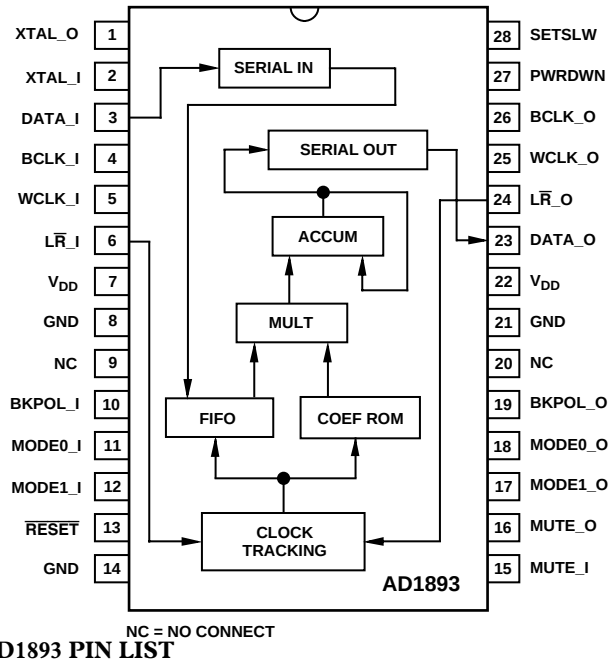
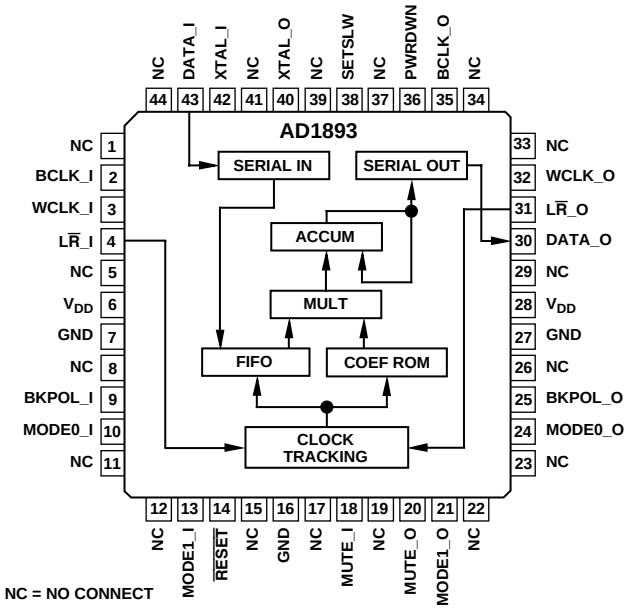
## PIN CONFIGURATIONS

**DIP**




NC = NO CONNECT

**LQFP**




NC = NO CONNECT

### AD1893 PIN LIST

**Serial Input Interface**

| Pin Name | DIP | LQFP | I/O | Description |
|---|---|---|---|---|
| DATA_I | 3 | 43 | I | Serial input, MSB first, containing two channels of 4 to 16 bits of twos-complement data per channel. |
| BCLK_I | 4 | 2 | I | Bit clock input for input data. Need not run continuously; may be gated or used in a burst fashion. |
| WCLK_I | 5 | 3 | I | Word clock input for input data. This input is rising edge sensitive. (Not required in LR input data clock triggered modes.) |
| LR_I | 6 | 4 | I | Left/right clock input for input data. Must run continuously. |

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**Serial Output Interface**

| Pin Name | DIP | LQFP | I/O | Description |
|---|---|---|---|---|
| DATA_O | 23 | 30 | O | Serial output, MSB first, containing two channels of 4- to 24-bits of twos-complement data per channel. |
| BCLK_O | 26 | 35 | I | Bit clock input for output data. Need not run continuously; may be gated or used in a burst fashion. |
| WCLK_O | 25 | 32 | I | Word clock input for output data. This input is rising edge sensitive. (Not required in LR output data clock triggered modes.) |
| LR_O | 24 | 31 | I | Left/right clock input for output data. Must run continuously. |

**Input Control Signals**

| Pin Name | DIP | LQFP | I/O | Description |
|---|---|---|---|---|
| BKPOL_I | 10 | 9 | I | Bit clock polarity. LO: Normal mode. Input data is sampled on rising edges of BCLK_I. HI: Inverted mode. Input data is sampled on falling edges of BCLK_I. |
| MODE0_I | 11 | 10 | I | Serial mode zero control for input port. |
| MODE1_I | 12 | 13 | I | Serial mode one control for input port. |

| MODE0_I | MODE1_I | |
|---|---|---|
| 0 | 0 | Left-justified, no MSB delay, LR_I clock triggered. |
| 0 | 1 | Left-justified, MSB delay, LR_I clock triggered. |
| 1 | 0 | Right-justified, MSB delayed 16 bit clock periods from LR_I transition. |
| 1 | 1 | WCLK_I triggered, no MSB delay. |

**Output Control Signals**

| Pin Name | DIP | LQFP | I/O | Description |
|---|---|---|---|---|
| BKPOL_O | 19 | 25 | I | Bit clock polarity. LO: Normal mode. Output data is valid on rising edges of BCLK_O, changed on falling. HI: Inverted mode. Output data is valid on falling edges of BCLK_O, changed on rising. |
| MODE0_O | 18 | 24 | I | Serial mode zero control for output port. |
| MODE1_O | 17 | 21 | I | Serial mode one control for output port. |

| MODE0_O | MODE1_O | |
|---|---|---|
| 0 | 0 | Left-justified, no MSB delay, $L\overline{R}$_O clock triggered. |
| 0 | 1 | Left-justified, MSB delay, $L\overline{R}$_O clock triggered. |
| 1 | 0 | Right-justified, MSB delayed 16 bit clock periods from $L\overline{R}$_O transition. |
| 1 | 1 | WCLK_O triggered, no MSB delay. |

**Miscellaneous**

| Pin Name | DIP | LQFP | I/O | Description |
|---|---|---|---|---|
| XTAL_O | 1 | 40 | O | Crystal output. Connect to one side of nominal 16 MHz crystal for sampling frequencies ($F_S$ word rates) from 8 kHz to 56 kHz. |
| XTAL_I | 2 | 42 | I | Crystal input. Connect to other side of nominal 16 MHz crystal for sampling frequencies ($F_S$ word rates) from 8 kHz to 56 kHz. Use this input to overdrive the on-chip oscillator with an external clock source. |
| $\overline{\text{RESET}}$ | 13 | 14 | I | Active LO reset. Set HI for normal chip operation. |
| MUTE_O | 16 | 20 | O | Mute output. HI indicates that data is not currently valid due to read and write FIFO memory pointer overlap. LO indicates normal operation. |
| MUTE_I | 15 | 18 | I | Mute input. HI mutes the serial output to zeros (midscale). Normally connected to MUTE_O. Reset LO for normal operation. |
| SETLSLW | 28 | 38 | I | Settle slowly to changes in sample rates. HI: Slow-settling mode (≈800 ms). Less sensitive to sample clock jitter. LO: Fast-settling mode (≈200 ms). Some narrow-band noise modulation may result from jitter on the $L\overline{R}$ clocks. This signal may be asynchronous with respect to the crystal frequency, and dynamically changed, but is normally pulled up or pulled down on a static basis. |
| PWRDWN | 27 | 36 | I | Power-down input. Set HI for inactive, low power dissipation state. Reset LO for normal operation. |
| NC | 9, 20 | 1, 5, 8, 11, 12, 15, 17, 19, 22, 23, 26, 29, 33, 34, 37, 39, 41, 44 | | No connect. Reserved. Do not connect. |

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**Power Supply Connections**

| Pin Name | DIP | LQFP | I/O | Description |
|---|---|---|---|---|
| $V_{DD}$ | 7, 22 | 6, 28 | I | Positive digital voltage supply. |
| GND | 8, 14, 21 | 7, 16, 27 | I | Digital ground. Pin 14 (DIP) and Pin 16 (LQFP) need not be decoupled. |

## THEORY OF OPERATION

There are at least two logically equivalent methods of explaining the concept of asynchronous sample rate conversion: the high speed interpolation/decimation model and the polyphase filter bank model. Using the AD1893 SamplePort does not require understanding either model. This section is included for those who wish a deeper understanding of its operation.

### Interpolation/Decimation Model

In the high speed interpolation/decimation model, illustrated in Figure 1, the sampled data input signal (Plot A in Figure 1) is interpolated at some ratio (IRATIO) by inserting IRATIO-1 zero valued samples between each of the original input signal samples (Plot B in Figure 1). The frequency domain characteristics of the input signal are unaltered by this operation, except that the zero-padded sequence is considered to be sampled at a frequency which is the product of original sampling frequency multiplied by IRATIO.

The zero-padded values are fed into a digital FIR low-pass filter (Plot C in Figure 1) to smooth or integrate the sequence, and limit the bandwidth of the filter output to 20 kHz. The interpolated output signal has been quantized to a much finer time scale than the original sequence. The interpolated sequence is then passed to a zero-order hold functional block (physically implemented as a register, Plot D in Figure 1) and then asynchronously resampled at the output sample frequency (Plot E in Figure 1). This resampling can be thought of as a decimation operation since only a very few samples out of the great many interpolated samples are retained. The output values represent the "nearest" values, in a temporal sense, produced by the interpolation operation. There is always some error in the output sample amplitude due to the fact that the output sampling switch does not close at a time that exactly corresponds to a point on the fine time scale of the interpolated sequence. However, this error can be made arbitrarily small by using a very large interpolation ratio. The AD1893 SamplePort ASRC uses an equivalent IRATIO of 65,536 to provide 16-bit accuracy (≈–96 dB THD+N) across the 0 kHz to 20 kHz audio band.

The number of FIR filter taps and associated coefficients is approximately 4 million. The equivalent FIR filter convolution frequency (or "upsample" frequency) is 3.2768 GHz, and the fine time scale has resolution of about 300 ps. Various proprietary efficiencies are exploited in the AD1893 ASRC to reduce the complexity and throughput requirements of the hardware implied by this interpolation/decimation model.

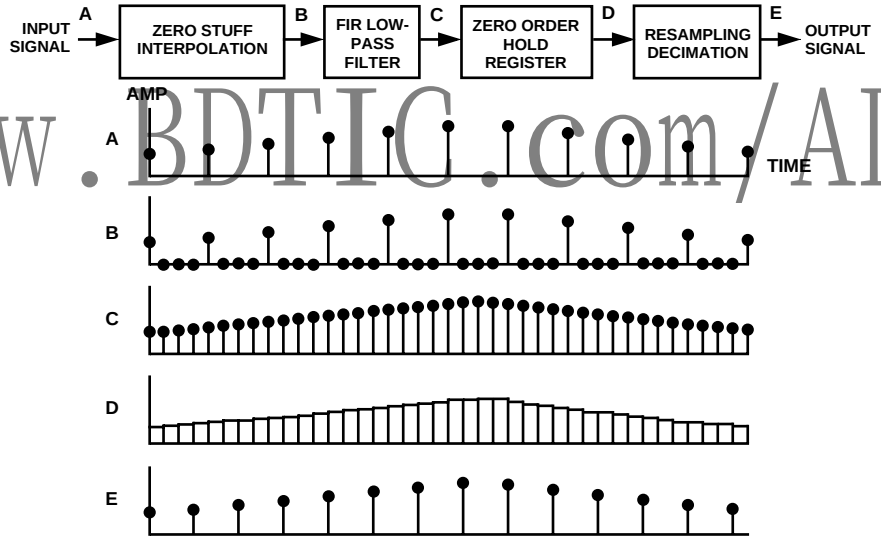


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*Figure 1. Interpolation/Decimation Model—Time Domain View*

**Polyphase Filter Bank Model**

Although less intuitively understandable than the interpolation/decimation model, the polyphase filter bank model is useful to explore because it more accurately portrays the operation of the actual AD1893 SamplePort hardware. In the polyphase filter bank model, the stored FIR filter coefficients are thought of as the impulse response of a highly oversampled 0 kHz to 20 kHz low-pass prototype filter, as shown in Figure 2. If this low-pass filter is oversampled by a factor of N, then it can be conceptually decomposed into N different "subfilters," each filter consisting of a different subset of the original set of impulse response samples. If the temporal position of each of the subfilters is maintained, then they can be summed to recreate the original oversampled impulse response. Since the original impulse response is highly oversampled, the more sparsely sampled subfilters still individually meet the Nyquist criterion (i.e., they are adequately sampled). The baseband magnitude and phase responses of the subfilters are identical. The out-of-band (i.e., alias) regions of the subfilters however have phase responses which are shifted relative to one another, in a manner that causes them to cancel when they are summed.

The subfilter coefficients are then aligned to the left, as shown in Figure 3, so that the first coefficient of each subfilter is aligned to the first point on a coarse time scale. (This conceptual step accounts for how the hardware implementation is able to operate at the slower rate corresponding to the coarse time scale.) Each subfilter has been shifted in time by a different amount, and though they still share identical magnitude responses, they now have in-band phase responses which have fractionally different slopes (i.e., group delays).

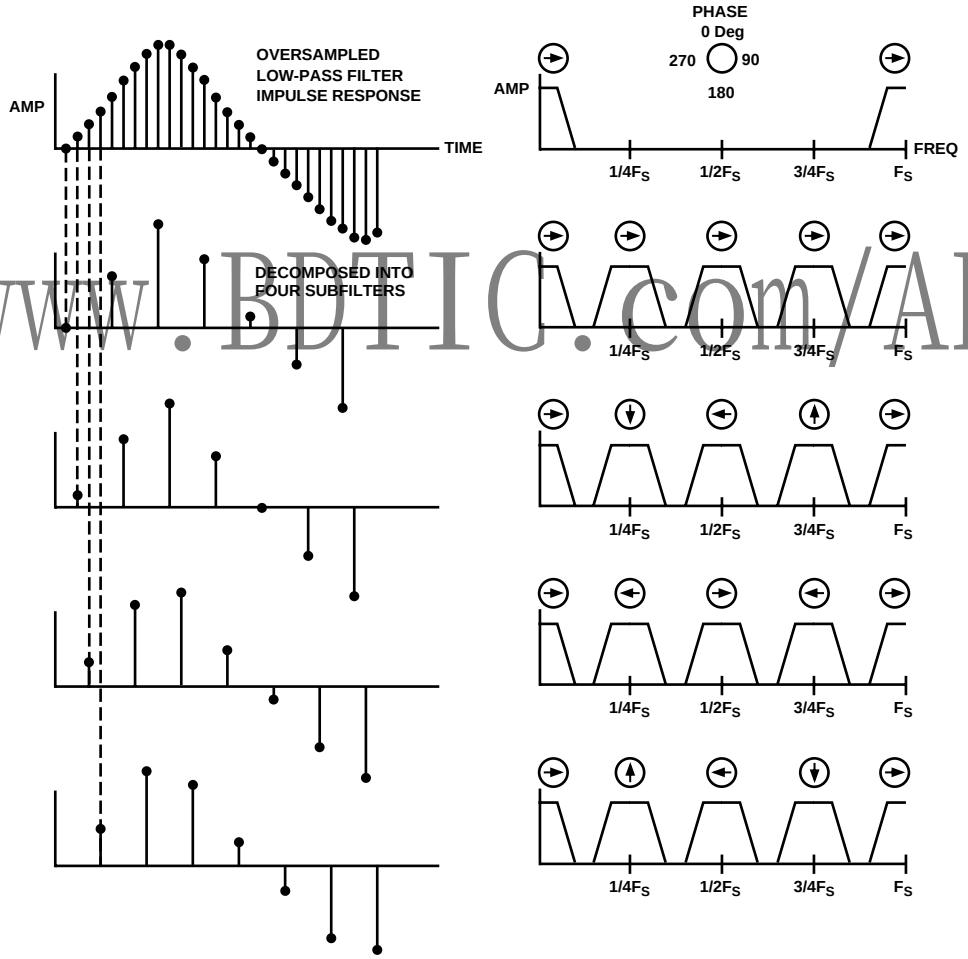


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*Figure 2. Four Polyphase Subfilters in the Time and Frequency Domains*

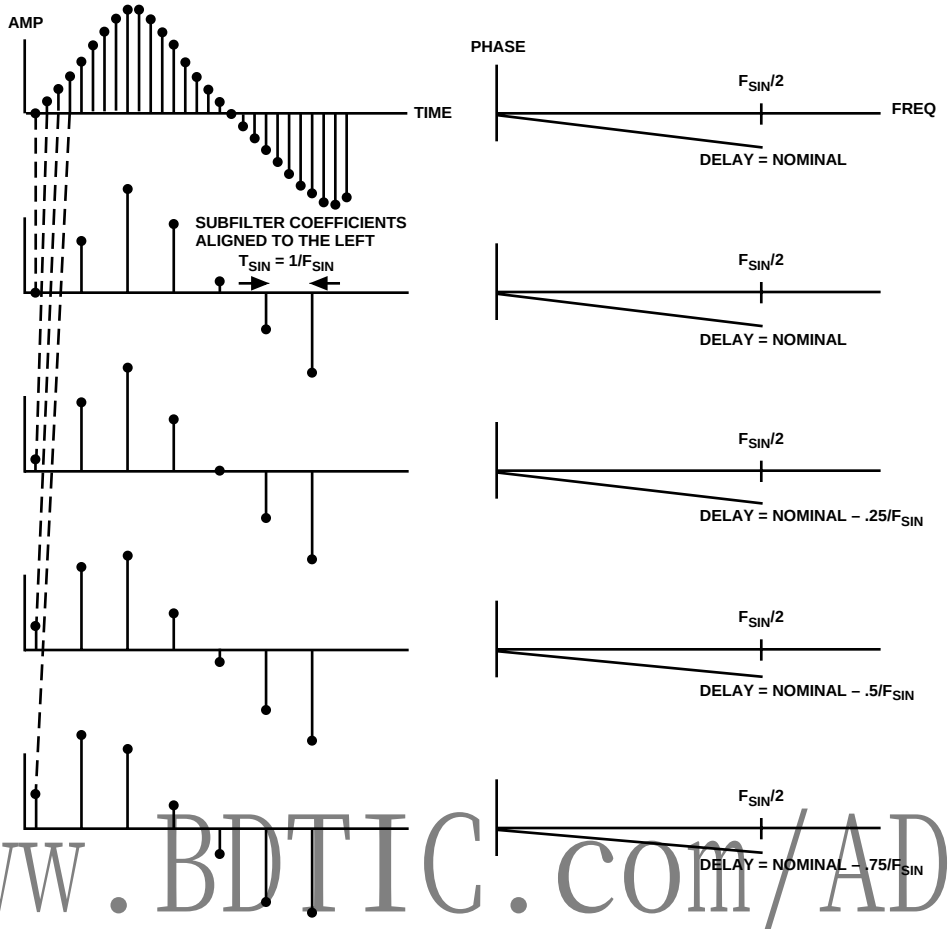


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*Figure 3. Four Polyphase Subfilters Realigned to Coarse Time Grid*

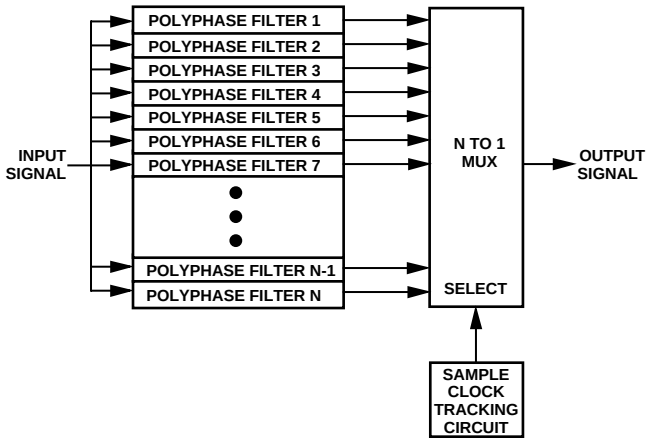


*Figure 4. Polyphase Filter Bank Model—Conceptual Block Diagram*

The full set of subfilters can be considered to form a parallel bank of "polyphase" filters which have decrementing, linear phase group delays. All of the polyphase filters conceptually process the input signal simultaneously, as illustrated in Figure 4, at the input sample rate.

Asynchronous sample rate conversion under the polyphase filter bank model is accomplished by selecting the output of a particular polyphase filter on the basis of the temporal relationship between the input sample clock and the output sample clock events. Figure 5 shows the desired filter group delay as a function of the relative time difference between the current output sample clock and the last input sample clock. If an output sample is requested late in the input sample period, then a short filter delay is required, and if an output sample is requested early in the input sample period, then a long filter delay is required. This nonintuitive result arises from the fact that FIR filters always produce some delay, so that selecting a filter with shorter delay moves the interpolated sample closer to the newest input sample.

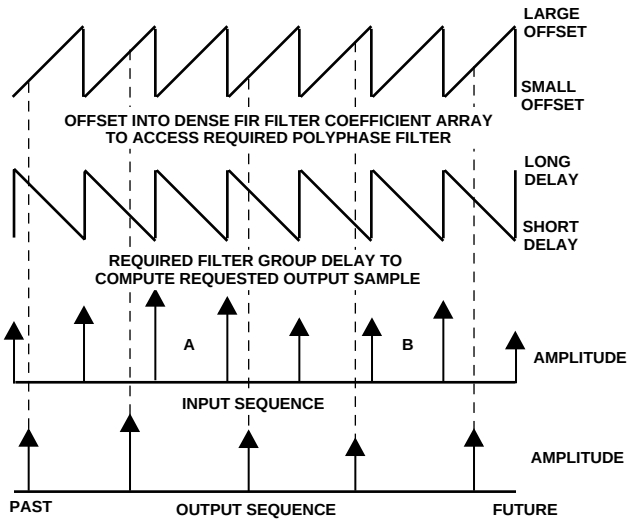


*Figure 5. Input and Output Clock Event Relationship*

A short delay corresponds to a large offset into the dense FIR filter coefficient array, and a long delay corresponds to a small offset. Note that because the output sample clock can arrive at any arbitrary time with respect to the input sample clock, the selection of a polyphase filter with which to convolve the input sequence occurs on every output sample clock event. Occasionally the FIFO which holds the input sequence in the FIR convolver is either not incremented, or incremented by two between output sample clocks (see periods A and B in Figure 5); this happens more often when the input and output sample clock frequencies are dissimilar than when they are close together. However, in this situation, an appropriate polyphase filter is selected to process the input signal, and thus an accurate output sample is computed. Input and output samples are not skipped or repeated (unless the input FIFO underflows or overflows), as is the case in some other sample rate converter implementations.

To obtain an accurate conversion, a large number of polyphase filters are needed. The AD1893 SamplePort uses the equivalent of 65,536 polyphase filters to achieve its high quality distortion and dynamic range specifications.

**Sample Clock Tracking**

It should be clear that, in either model, the correct computation of the ratio between the input sample rate (as determined from the left/right input clock, LR_I) and the output sample rate (as determined from the left/right output clock, LR_O) is critical to the quality of the output data stream. It is straightforward to compute this ratio if the sample rates are fixed and synchronous; the challenge is to accurately track dynamically varying and asynchronous sample rates, as well as to account for jitter.

The AD1893 SamplePort solves this problem by embedding the ratio computation circuit within a digital servo control loop, as shown in Figure 6. This control loop includes special provisions to allow for the accurate tracking of dynamically changing sample rates. The outputs of the control loop are the starting read addresses for the input data FIFO and the filter coefficient ROM. These start addresses are used by the FIFO and ROM address generators, as shown in Figure 6.

The input data FIFO write address is generated by a counter which is clocked by the input sample clock (i.e., LR_I). It is very important that the FIFO read address and the FIFO write address do not cross, as this means that the FIFO has either underflowed or overflowed. This consideration affects the choice of settling time of the control loop. When a step change in the sample rate occurs, the relative positions of the read and write addresses will change while the loop is settling. A fast settling loop will act to keep the FIFO read and write addresses separated better than a slow settling loop. The AD1893 includes a user selectable pin (SETLSLW) to set the loop settling time that essentially changes the coefficients of the digital servo control loop filter. The state of the SETLSLW pin can be changed on-the-fly but is normally set and forgotten.

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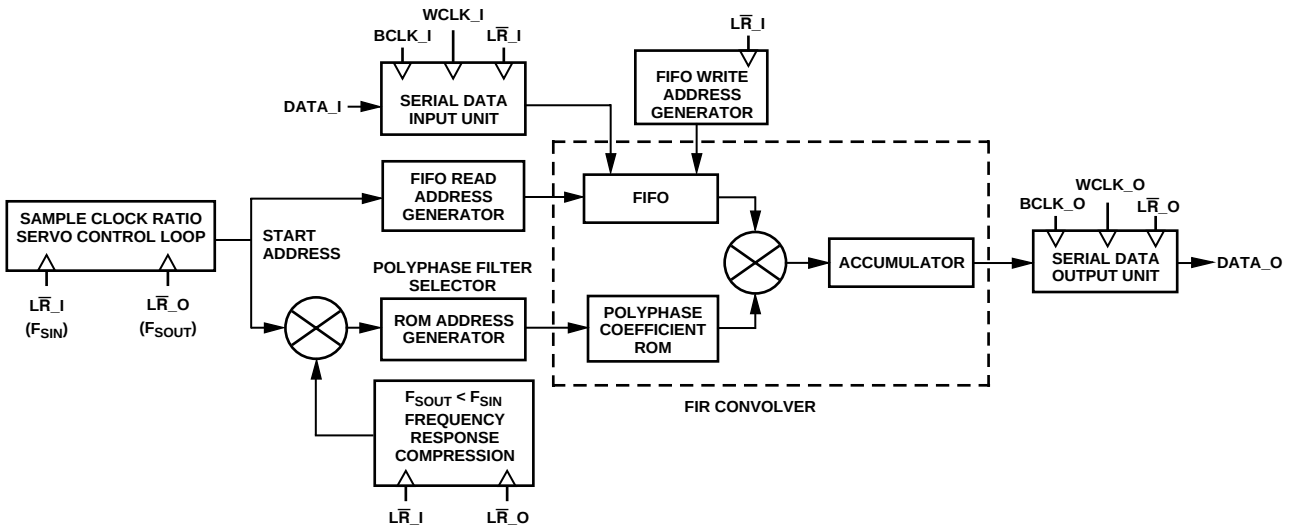


*Figure 6. Functional Block Diagram*

**Sample Clock Jitter Rejection**

The loop filter settling time also affects the ability of the AD1893 ASRC to reject sample clock jitter, since the control loop effectively computes a time weighted average or "estimated" new output of many past input and output clock events. This first order low pass filtering of the sample clock ratio provides the AD1893 with its jitter rejection characteristic. In the slow settling mode, the AD1893 attenuates jitter frequencies higher than 3 Hz (≈800 ms for the control loop to settle to an 18-bit "pure" sine wave), and thus rejects all but the most severe sample clock jitter; performance is essentially limited only by the FIR filter. In the fast settling mode, the ASRC attenuates jitter components above 12 Hz (≈200 ms for the control loop to settle). Due to the effects of on-chip synchronization of the sample clocks to the 16 MHz (62.5 ns) crystal master clock, sample clock jitter must be a large percentage of the crystal period (>10 ns) before performance degrades in either the slow or fast settling modes. Note that since both past input and past output clocks are used to compute the filtered "current" internal output clock request, jitter on both the input sample clock and the output sample clock is rejected equally. In summary: the fast-settling mode is best for applications when the sample rates will be dynamically altered (e.g., varispeed situations), while the slow-settling mode provides the most sample clock jitter rejection.

Clock jitter can be modeled as a frequency modulation process. Figure 7 shows one such model, where a noise source combined with a sine wave source modulates the "carrier" frequency generated by a voltage controlled oscillator.

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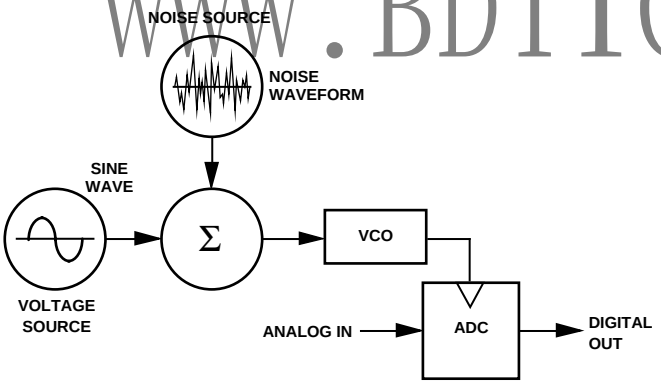


*Figure 7. Clock Jitter Modeled as a Modulated VCO*

If the jittered output of the VCO is used to clock an analog-to-digital converter, the digital output of the ADC will be contaminated by the presence of jitter. If the noise source is spectrally flat (i.e., "white" jitter), an FFT of the ADC digital output would show a spectrum with a uniform noise floor that is elevated compared to the spectrum with the noise source turned off. If the noise source has distinct frequency components (i.e., "correlated" jitter), then an FFT of the ADC digital output would show symmetrical sidebands around the ADC input signal, at amplitudes and frequencies determined by frequency modulation theory. One notable result is that the level of the noise or the sidebands is proportional to the slope of the input signal, i.e., the worst case occurs at the highest frequency full-scale input (a full-scale 20 kHz sinusoid).

The AD1893 applies rejection to these jitter frequency components referenced to the input signal. In other words, if a 5 kHz digital sinusoid is applied to the ASRC, depending on the settling mode selected, the ASRC will attenuate sample clock jitter at either 3 Hz above and below 5 kHz (slow settling) or 12 Hz above and below 5 kHz (fast settling). The rolloff is 6 dB per octave. As an example, suppose there was correlated jitter present on the input sample clock with a 1 kHz component, associated with the same 5 kHz sinusoidal input data. This would produce sidebands at 4 kHz and 6 kHz, 3 kHz and 7 kHz, etc., with amplitudes that decrease as they move away from the input signal frequency. For the slow-settling mode case, 1 kHz represents more than nine octaves (relative to 3 Hz), so the first two sideband pairs would be attenuated by more than 54 dB. For the fast-settling mode case, 1 kHz represents more than seven octaves (relative to 12 Hz), so that the first two sideband pairs would be attenuated by more than 42 dB. The second and higher sideband pairs are attenuated even more because they are spaced further from the input signal frequency.

**Group Delay Modes**

The other parameter that determines the likelihood of FIFO input overflow or output underflow is the FIFO depth. This FIFO induced group delay is better termed transport delay, since it is frequency independent, and should be kept conceptually distinct from the notion of group delay as used in the polyphase filter bank model. The total group delay of the AD1893 equals the FIFO transport delay plus the FIR (polyphase) filter group delay.

In the AD1893, the FIFO read and write pointers are separated by five memory locations (≈100 μs equivalent transport delay at a 50 kHz sample rate). This is added to the FIR filter delay (64 taps divided by 2) for a total nominal group delay in short mode of ≈700 μs.

This delay is deterministic and constant except when $F_{SOUT}$ drops below $F_{SIN}$ which causes the number of FIR filter taps to increase (see Cutoff Frequency Modification section). If the FIFO read and write addresses cross, the MUTE_O signal will be asserted. Note that under all conditions, both the highly oversampled low-pass prototype and the polyphase subfilters of the AD1893 ASRC possess a linear phase response.

**Cutoff Frequency Modification**

The final important operating concept of the ASRC is the modification of the filter cutoff frequency when the output sample rate ($F_{SOUT}$) drops below the input sample rate ($F_{SIN}$), i.e., during downsampling operation. The AD1893 automatically reduces the polyphase filter cutoff frequency under this condition. This lowering of the cutoff frequency (i.e., the reduction of the input signal bandwidth) is required to avoid alias distortion. The AD1893 SamplePort takes advantage of the scaling property of the Fourier transform which can be stated as follows: if the Fourier transform of f(t) is F(w), then the Fourier transform of f(k × t) is F(w/k). This property can be used to linearly compress the frequency response of the filter, simply by multiplying the coefficient ROM addresses (shown in Figure 6) by the ratio of $F_{SOUT}$ to $F_{SIN}$ whenever $F_{SOUT}$ is less than $F_{SIN}$. This scaling property works without spectral distortion because the time scale of the interpolated signal is so dense (300 ps resolution) with respect to the cutoff frequency that the discrete-time representation is a close approximation to the continuous time function.

The cutoff frequency (–3 dB down) of the FIR filter during downsampling is given by the following relation:

$$\textit{Downsampling Cutoff Frequency} = (F_{SOUT}/44.1\ kHz) \times 20\ kHz$$

The AD1893 frequency response compression circuit includes a first order low-pass filter to smooth the filter cutoff frequency selection during dynamic sample rate conditions. This allows the ASRC to avoid objectionable clicking sounds that would otherwise be imposed on the output while the loop settles to a new sample rate ratio. Hysteresis is also applied to the filter selection with approximately 300 Hz of cutoff frequency "noise margin," which limits the available selection of cutoff frequencies to those falling on an approximately 300 Hz frequency grid. Thus if a particular sample frequency ratio was reached by sliding the output sample frequency up, it is possible that a filter will be chosen with a cutoff frequency that could differ by as much as 300 Hz from the filter chosen when the same sample frequency ratio was reached by sliding the output sample frequency down. This is necessary to ensure that the filter selection is stable even with severely jittered input sample clocks.

Note that when the filter cutoff frequency is reduced, the transition band of the filter becomes narrower since the scaling property affects all filter characteristics. The number of FIR filter taps necessarily increases because there are now a smaller number of longer length polyphase filters. Nominally, when $F_{SOUT}$ is greater than $F_{SIN}$, the number of taps is 64. When $F_{SOUT}$ is less than $F_{SIN}$, the number of taps linearly increase to a maximum of 128 when the ratio of $F_{SOUT}$ to $F_{SIN}$ equals 1:2. The number of filter taps as a function of sample clock ratio is illustrated in Figure 8. The natural consequence of this increase in filter taps is an increase in group delay.

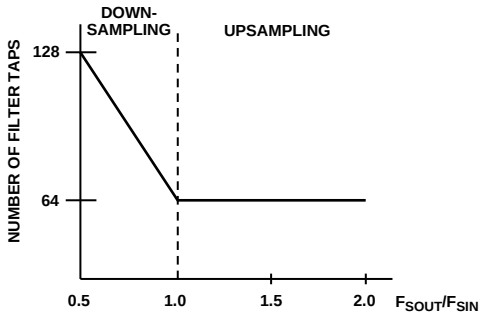


*Figure 8. Number of Filter Taps as a Function of $F_{SOUT}/F_{SIN}$*

When the AD1893 output sample frequency is higher than the input sample frequency (i.e., upsampling operation), the cutoff frequency of the FIR polyphase filter can be greater than 20 kHz. The cutoff frequency of the FIR filter during upsampling is given by the following relation:

$$\textit{Upsampling Cutoff Frequency} = (F_{SIN}/44.1\ kHz) \times 20\ kHz$$

**Noise and Distortion Phenomena**

There are three noise/distortion phenomena that limit the performance of the AD1893 ASRC. First, there is broadband, Gaussian noise that results from polyphase filter selection quantization. Even though the AD1893 has a large number of polyphase filters (the equivalent of 65,536) from which to choose, the selection is not infinite. Second, there is narrowband noise that results from the nonideal synchronization of the sample clocks to the 16 MHz system clock, which leads to a nonideal computation of the sample clock ratio, which leads to a nonideal polyphase filter selection. This noise source is narrowband because the digital servo control loop averages the polyphase filter selection, leading to a strong correlation between selections from output to output. In slow mode, the selection of polyphase filters is completely unaffected by the clock synchronization. In fast mode, some narrowband noise modulation may be observed with very long FFT measurements. This situation is analogous to the behavior of a phase locked loop when presented with a noisy or jittered input. Third, there are distortion components that are due to the noninfinite stopband rejection of the low-pass filter response. Noninfinite stopband rejection means that some amount of out-of-band spectral energy will alias into the baseband. The AD1893 performance specifications include the effects of these phenomena.

Note that Figures 16 through 18 are shown with full-scale input signals. The distortion and noise components will scale with the input signal amplitude. In other words, if the input signal is attenuated by –20 dB, the distortion and noise components will also be attenuated by –20 dB. This dependency holds until the effects of the 16-bit input quantization are reached.

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## OPERATING FEATURES

### Serial Input/Output Ports

The AD1893 uses the frequency of the left/right input clock (LR_ I) and the left/right output clock (LR_O) signals to determine the sample rate ratio, and therefore these signals must run continuously and transition twice per sample period. (The LR_I clock frequency is equivalent to $F_{SIN}$ and the LR_O clock frequency is equivalent to $F_{SOUT}$.) The other clocks (WCLK_I, WCLK_O, BCLK_I, BCLK_O) are edge sensitive and may be used in a gated or burst mode (i.e., a stream of pulses during data transmission or reception followed by periods of inactivity). The word clocks and the output bit clock are used only to write data into or read data out of the serial ports; only the left/right clocks are used in the internal DSP blocks. The input bit clock is used to sample the input left/right clock. It is important that the left/right clocks are "clean" with monotonic rising and falling edge transitions and no excessive overshoot or undershoot which could cause false triggering on the AD1893.

The AD1893's flexible serial input and output ports consume and produce data in twos-complement, MSB-first format. The left channel data field always precedes the right channel data field; the current channel being consumed or produced is indicated by the state of the left/right clock (LR_I and LR_O). A left channel field, right channel field pair is called a frame. The input data field consists of 4 to 16 bits. The output data field consists of 4 to 24 bits. The input signals are specified to TTL logic levels, and the outputs swing to full CMOS logic levels. The ports are configured by pin selections.

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### Serial I/O Port Modes

The AD1893 has pin-selectable bit clock polarity for the input and output ports. In "normal" mode (BKPOL_I or BKPOL_O LO) the data is valid on the rising edge. In the "inverted" mode (BKPOL_I or BKPOL_O HI) the data is valid on the falling edge. Both modes are shown in Figures 23 and 24.

The AD1893 uses two multiplexed input pins to control the mode configuration of the input and output serial ports. MODE0_I and MODE1_I control the input serial port, and MODE0_O and MODE1_O control the output serial port as follows:

| MODE0_I | MODE1_I | Serial Input Port Mode |
|---|---|---|
| 0 | 0 | Left-justified, no MSB delay, LR_I clock triggered. |
| 0 | 1 | Left-justified, MSB delay, LR_I clock triggered. |
| 1 | 0 | Right-justified, MSB delayed 16-bit clock periods from LR_I clock transition, LR_I clock triggered. |
| 1 | 1 | Word clock triggered, no MSB delay. |

| MODE0_O | MODE1_O | Serial Output Port Mode |
|---|---|---|
| 0 | 0 | Left-justified, no MSB delay, LR_O clock triggered. |
| 0 | 1 | Left-justified, MSB delay, LR_O clock triggered. |
| 1 | 0 | Right-justified, MSB delayed 16-bit clock periods from LR_O clock transition, LR_O clock triggered. |
| 1 | 1 | Word clock triggered, no MSB delay. |

The MSB delay is useful for $I^2S$ format compatibility and for ease of interfacing to some DSP processors.

The AD1893 SamplePort serial ports operate in either the word clock (WCLK_I, WCLK_O) triggered mode or left/right clock (LR_I, LR_O) triggered mode. These modes can be utilized independently for the input and output ports. In the word clock triggered mode, as shown in Figure 23, after the left/right clock is valid, the appearance of the MSB of data is synchronous with the rising edge of the word clock. Note that the word clock is rising edge sensitive, and can fall anytime after it is sampled HI by the bit clock. In the left-justified left/right clock triggered modes, as shown in Figure 24, the appearance of the MSB of data is synchronous with the rising edge of the left/right clock for the left channel and the falling edge of left/right clock for the right channel. The MSB is delayed by one bit clock after the left/right clock if the MSB delay mode is selected. In the right-justified left/right clock triggered mode, as shown in Figure 25, the MSB is delayed 16 bit clock periods from a left/right clock edge, so that when there are 64 bit clock periods per frame, the LSB is right-justified to a left/right clock edge. The word clock is not required in the left/right clock triggered modes, and should be tied either HI or LO. Figure 24 shows the bit clock in the optional gated or burst mode; the bit clock is inactive between data fields, and can take either the HI state or the LO state while inactive.

Note that there is no requirement for a delay between the left channel data and the right channel data. The left/right clocks and the word clocks can transition immediately after the LSB of the data, so that the MSB of the subsequent channel appears without any timing delay. The AD1893 is therefore capable of a 32-bit frame mode, in which both 16-bit channels are packed into a 32-bit clock period. More generally, there is no particular requirement for when the left/right clock falls (i.e., there is no left/right clock duty cycle or pulsewidth specification), provided that the left/right clock frequency equals the intended sample frequency, and there are sufficient bit clock periods to clock in or out the intended number of data bits.

### On-Chip Oscillator

The AD1893 includes an on-chip oscillator so that the user need only supply an external quartz crystal or ceramic resonator. The crystal or the resonator should be tied to the XTAL_I and XTAL_O pins of the AD1893. An external crystal oscillator can be used to overdrive the AD1893 on-chip oscillator. The external clock source should be applied to the XTAL_I pin, and the XTAL_O pin should be left unconnected.

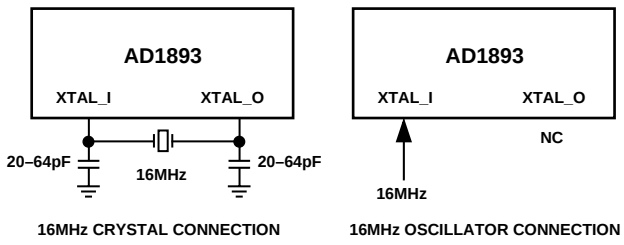


*Figure 9. Crystal and Oscillator Connections*

Some applications using multiple AD1893s may desire to use the same master clock frequency for all the SamplePorts, supplied by a single crystal. The crystal output can be buffered with a 74HCXX gate and distributed to the other XTAL_I inputs, as shown in Figure 10.

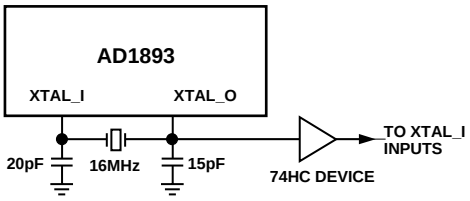


*Figure 10. Buffered 16 MHz Crystal Connection*

**Power-Down Mode**

The AD1893 includes a power-down control input pin PWRDWN. This control signal is active HI, and puts the AD1893 in an inactive state with very low power dissipation. The PWRDWN pin should be connected LO when normal operation of the AD1893 is desired.

**Control Signals**

The SETLSLW, BKPOL_I, BKPOL_O, MODE0_I, MODE1_I, MODE0_O and MODE1_O inputs are asynchronous signals in that they need obey no particular timing relation to the crystal frequency or the sample clocks. Ordinarily, these pins are hardwired or connected to an I/O register for microprocessor control. The only timing requirement on these pins is that the control signals are stable and valid before the first serial input data bit (i.e., the MSB) is presented to the AD1893.

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**Reset**

Figure 27 shows the reset timing for the AD1893 SamplePort. A crystal (or resonator) must be connected to the AD1893 when $\overline{\text{RESET}}$ is asserted, and the bit clocks, the word clocks and the left/$\overline{\text{right}}$ clocks may also be running. When the AD1893 comes out of reset, it defaults to a $F_{SIN}$ to $F_{SOUT}$ ratio of 1:1. The filter pipeline is not cleared. However, the mute output goes HI for at least 128 cycles, adequate to allow the pipeline to clear. If $F_{SIN}$ differs significantly from $F_{SOUT}$, then the AD1893 sample clock servo control loop also has to settle. While settling, the mute output will be HI. After the external system resets the AD1893, it should wait until the mute output goes LO before clocking in serial data.

There is no requirement for using the $\overline{\text{RESET}}$ pin at power-up or when the input or output sample rate changes. If it is not used, the AD1893 will settle to the sample clocks supplied within ≈200 ms in fast-settling mode or within ≈800 ms in slow-settling mode.

## APPLICATION ISSUES

**Dither**

Due to the large output word length, no redithering of the AD1893 output is necessary. This assumes that the input is properly dithered and the user retains the same or greater number of output bits as there are input bits. The AD1893 output bit stream may thus be used directly as the input to downstream digital audio processors, storage media or output devices.

If the AD1893 is to be used to dramatically downsample (i.e., output sample frequency is much lower than input sample frequency), the input should be sufficiently dithered to account for the limiting of the input signal bandwidth (which reduces the rms level of the input dither). No dither is internally used or applied to the audio data in the AD1893 SamplePort.

**Decoupling and PCB Layout**

The AD1893 ASRC has two power and two ground connections to minimize output switching noise and ground bounce. (Pins 14 [DIP] and 16 [LQFP] are actually control inputs, and should be tied LO, but need not be decoupled.) The DIP version places the power and ground pins at the center of the device to optimize switching performance. The AD1893 should be decoupled with two high quality 0.1 µF or 0.01 µF ceramic capacitors (preferably surface mount chip capacitors, due to their low inductance), one between each $V_{DD}$/GND pair. Best practice PCB layout and interconnect guidelines should be followed. This may include terminating the bit clocks or the left/$\overline{\text{right}}$ clocks if excessive overshoot or undershoot is evident and avoiding parallel PCB traces to minimize digital crosstalk between clocks and control lines. Note that DIP and LQFP sockets reduce electrical performance due to the additional inductance they impose; sockets should therefore be used only when required.

**Master Clock**

Using a 16 MHz crystal, the nominal range of sample frequencies that the AD1893 accepts is from 8 kHz to 56 kHz. Other sample frequency ranges are possible by linearly scaling the crystal frequency. For example, a 12 MHz crystal would yield a sample frequency range of 6 kHz to 42 kHz. The approximate relative upper bound sample frequency is the crystal frequency divided by 286; the approximate relative lower bound sample frequency is the crystal frequency divided by 2000. The audio performance will not degrade if the sample frequencies are kept within these bounds. The AD1893 SamplePort is production tested at 16 MHz. Note that due to finite register length constraints, there is a minimum input sample frequency ($\overline{\text{LR}}$_I). The allowable input and output sample frequency ranges for crystal frequencies of 16 MHz and 12 MHz are shown in Figures 11 and 12.

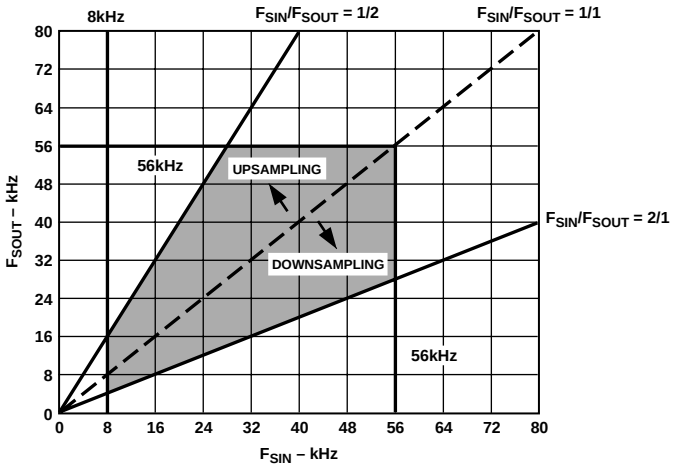


*Figure 11. Allowable Input and Output Sample Frequencies $F_{CRYSTAL}$ = 16 MHz Case*

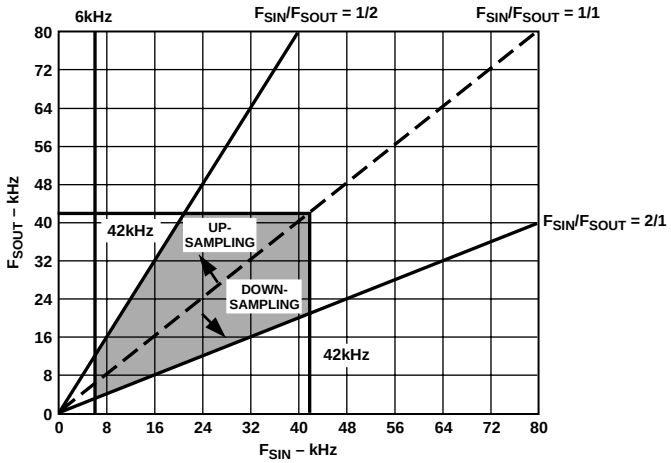


*Figure 12. Allowable Input and Output Sample Frequencies $F_{CRYSTAL}$ = 12 MHz Case*

**Multiple SamplePort Synchronization and Performance Degradation**

Multiple parallel AD1893 SamplePorts may be used in a single system. Multiple AD1893s can be "synchronized" by simply sharing the same reset and buffered crystal connections (see Figure 10), and ensuring that all the SamplePorts leave the reset state on the same crystal falling edge. No other provision is necessary since the different AD1893s will process samples identically if they are presented with the same input and output clocks (neglecting the effect of excessive clock skew on the PCB, as well process variations between ASRCs which could cause different devices to trigger at slightly different times on excessively slow rising or falling clock edges).

It is also likely that several AD1893s could end up in a serial cascade arrangement, either in a single system design or as the result of two or more systems, each using a single AD1893 in the signal path. The audio signal quality will be degraded with each pass through a SamplePort, though to a very minor degree. The THD+N performance will degrade by 3 dB with every doubling of the number of passes through an ASRC. For example, the AD1893 THD+N specification of –94 dB will rise to –91 dB if the signal makes two passes through an ASRC. The overall system THD+N specification will rise to –88 dB with four passes, and so on.

**Clipping**

Under certain rare input conditions, it is possible for the AD1893 to produce a clipped output sample. This situation is best comprehended by employing the interpolation/decimation model. If two consecutive samples happened to have full-scale amplitudes (representing the peak of a full-scale sine wave, for example), the interpolated sample (or samples) between these two samples might have an amplitude greater than full scale. As this is not possible, the AD1893 will compute a full-scale amplitude for the interpolated sample or samples (see Figure 13). Clipping can also arise due to the pre-echo and post-echo Gibbs phenomena of the FIR filter, when presented with a full-scale step input. The result of this erroneous or clipped output sample may be measured as an extremely small decrease in headroom for transient signals.

**Sample Rate Conversion Ratio Range**

The AD1893 does not support exact 1:2 (or 2:1) sample rate conversion. The SamplePort will convert to within several hertz of the 1:2 range, but will mute before reaching the exact 1:2 ratio. Thus the AD1893 will not support applications where the input and output sample clocks are derived from a common source but differ by a divide-by-two. When the ratio between the input and output sample clock reaches to within 1% of 1:2 or 2:1, the THD+N performance may degrade by several decibels, due to the wraparound of the internal read/write memory location pointers.

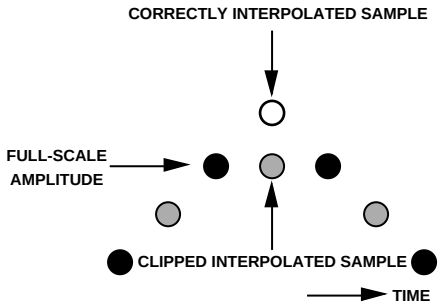


*Figure 13. Nipped Output Sample*

**Options for Sample Rate Conversion over a Wider Range**

There are systems requiring sample rate conversion over a range that is wider than the 1:2 or 2:1 range provided by a single AD1893, such as for "scrubbing" in digital audio editors. There are at least two options in this situation. The first is to use a programmable DSP chip to perform simple integer ratio interpolation or decimation, and then use the AD1893 when this intermediate output sample frequency is within the approximate 1:2 or 2:1 range of the final desired output sample frequency. The second is to use multiple AD1893 devices cascaded in series to achieve the required sample rate range.

**"Almost Synchronous" Operation**

It is possible to apply input and output sample frequencies which are very close (within a few hertz) or in fact synchronous ($\overline{LR}$_I and $\overline{LR}$_O tied together). There is no performance penalty when using the AD1893 in "almost synchronous" applications. Indeed, there is a very slight performance benefit when the input and output sample clocks are synchronous since the alias distortion components which arise from the noninfinite stopband attenuation of the FIR filter will pile up exactly on top of the sinusoidal frequency components of the input signal, and will thus be masked.

It has been empirically observed that during almost synchronous operation, certain AES/EBU receivers, when used to generate the input bit clock (BCLK_I) using a 128 times $F_S$ bit clock frequency, can suffer sympathetic phase lock to the output bit clock (BCLK_O) when the output bit clock is also operated at a 128 times $F_S$ rate. In other words, due to a noise pickup mechanism in the analog phase lock loop portion of these AES/EBU receivers, the lock frequency is pulled to match the frequency of the output bit clock. The system can suffer intermittent bursts of audible distortion when this sympathetic lock phenomenon occurs. Analog Devices recommends avoiding the use of a 128 times $F_S$ output bit clock frequency if almost synchronous application is intended. The use of a 64 times $F_S$ output bit clock rate is recommended.

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**System Mute**

The mute function applies to both right and left channels on the AD1893. The user can include a system-specific output mute signal, while retaining the automatic mute feature of the AD1893 by using the circuit shown in Figure 14.

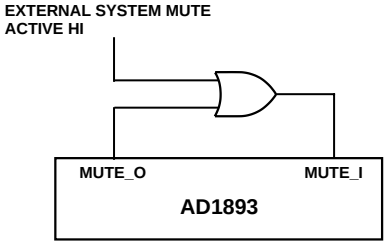


*Figure 14. External Mute Circuit*

## Performance Graphs

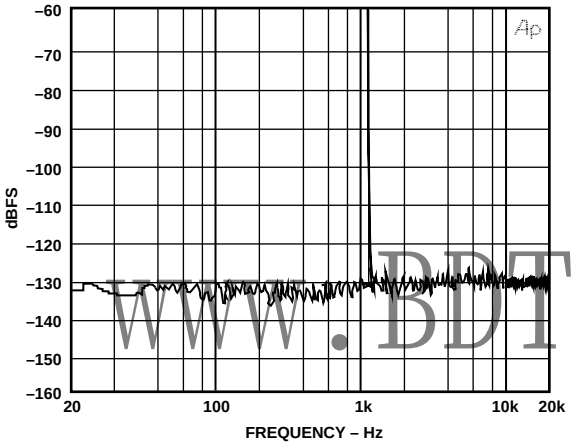


*Figure 15. Dynamic Range from 20 Hz to 20 kHz, –60 dBFS, 48 kHz Input Sample Frequency, 44.1 kHz Output Sample Frequency, 16k-Point FFT, BH4 Window*

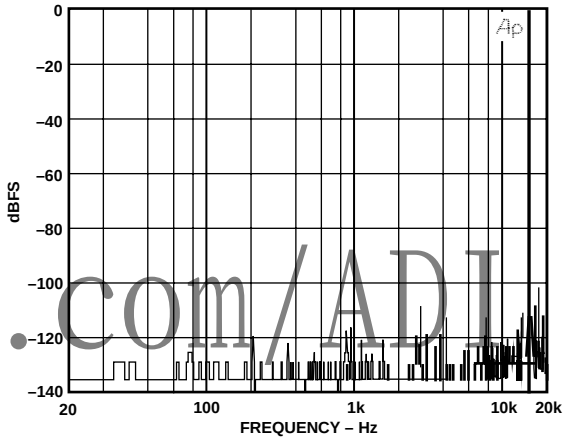


*Figure 17. 15 kHz Tone at 0 dBFS, 48 kHz Input Sample Frequency, 44.1 kHz Output Sample Frequency, 16k-Point FFT, BH4 Window*

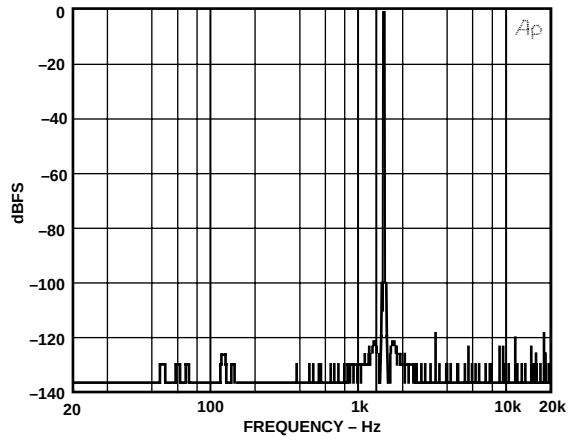


*Figure 16. 1 kHz Tone at 0 dBFS, 48 kHz Input Sample Frequency, 44.1 kHz Output Sample Frequency, 16k-Point FFT, BH4 Window*

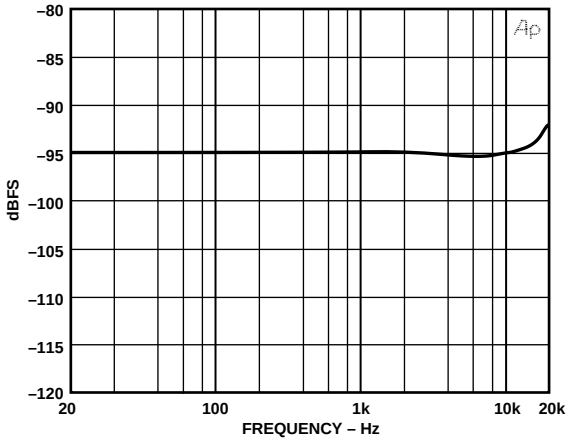


*Figure 18. THD+N vs. Frequency, 48 kHz Input Sample Frequency, 44.1 kHz Output Sample Frequency, Full-Scale Input Signal*

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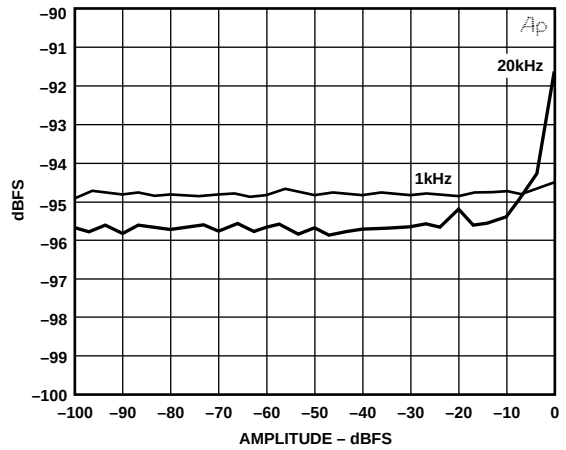


*Figure 19. THD+N vs. Input Amplitude, 44.1 kHz Input Sample Frequency, 48 kHz Output Sample Frequency, 1 kHz and 20 kHz Tones*

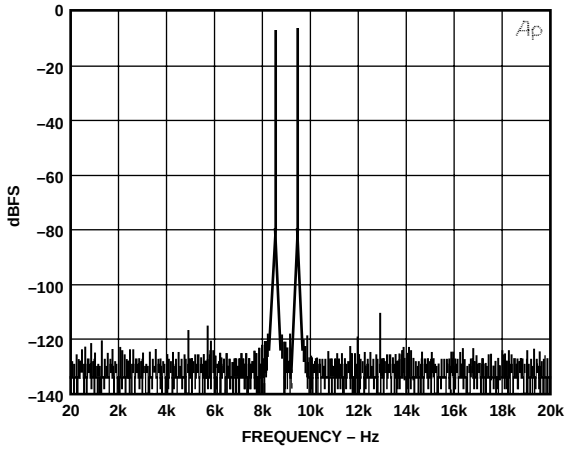


*Figure 21. Twintone, 10 kHz and 11 kHz, 44.1 kHz Input Sample Frequency, 48 kHz Output Sample Frequency, 16k-Point FFT, BH4 Window*

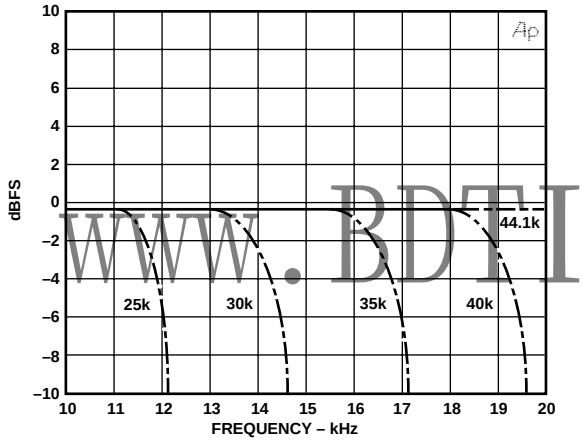


*Figure 20. Digital Filter Signal Transfer Function, 10 kHz to 20 kHz, 44.1 kHz Input Sample Frequency, 44.1, 40, 35, 30 and 25 kHz Output Sample Frequencies*

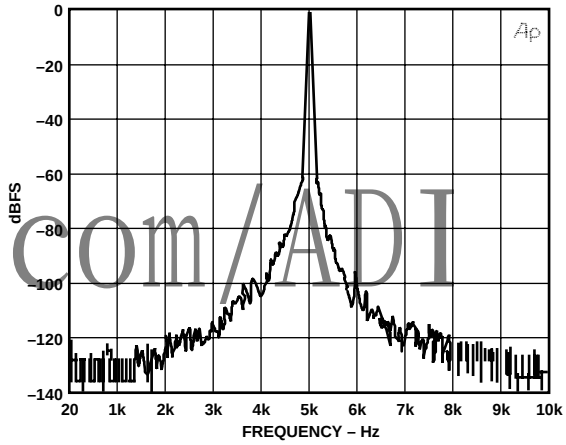


*Figure 22. 5 kHz Tone at 0 dBFS with 100 ns p-p Binominal Jitter on L/$\overline{R}$ Clocks, Fast Settling Mode, 48 kHz Input Sample Frequency, 44.1 kHz Output Sample Frequency, 16k-Point FFT, BH4 Window*

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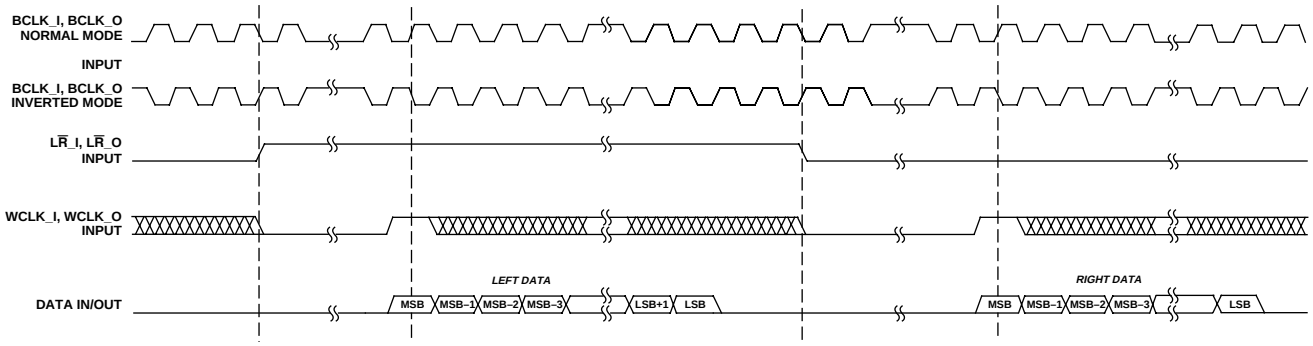


*Figure 23. Serial Data Input and Output Timing, Word Clock Triggered Mode*

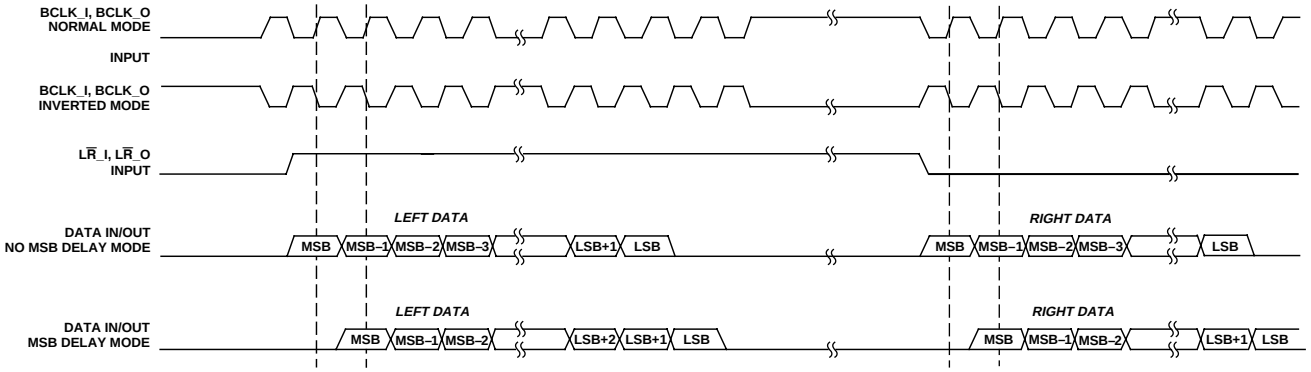


*Figure 24. Serial Data Input and Output Timing, Left-Justified Left/$\overline{\text{Right}}$ Clock Triggered Modes*

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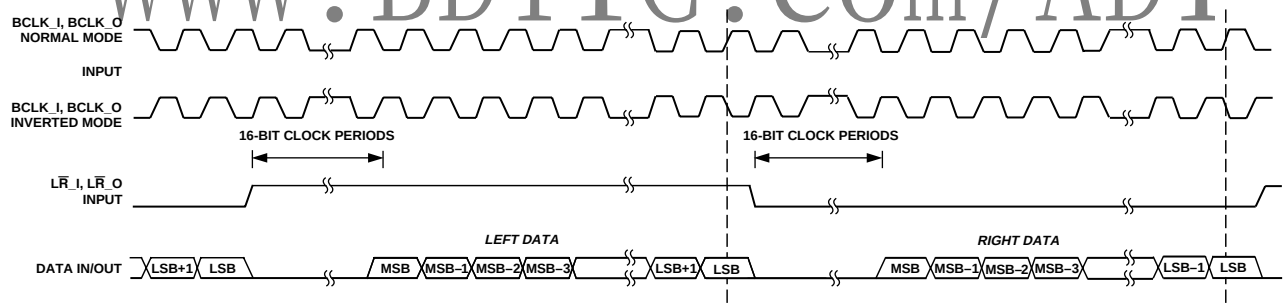


*Figure 25. Serial Data Input and Output Timing, Right-Justified Left/$\overline{\text{Right}}$ Clock Triggered Mode*

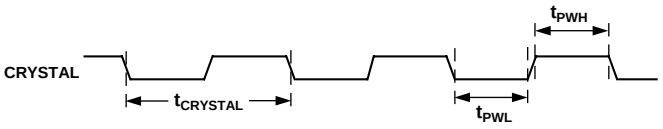


*Figure 26. Clock Timing*

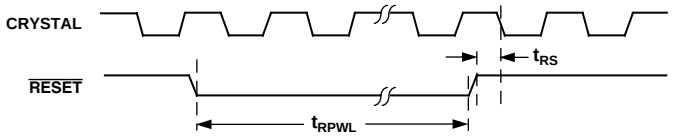


*Figure 27. Reset Timing*

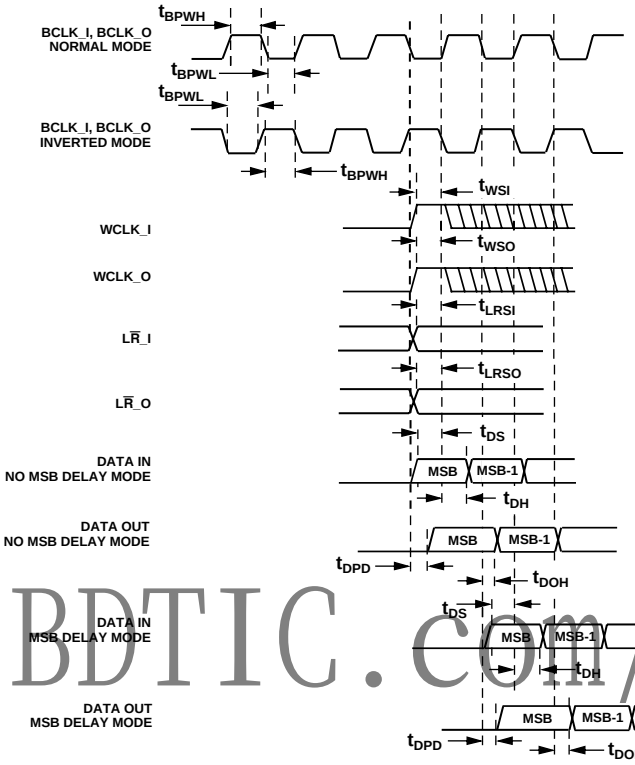


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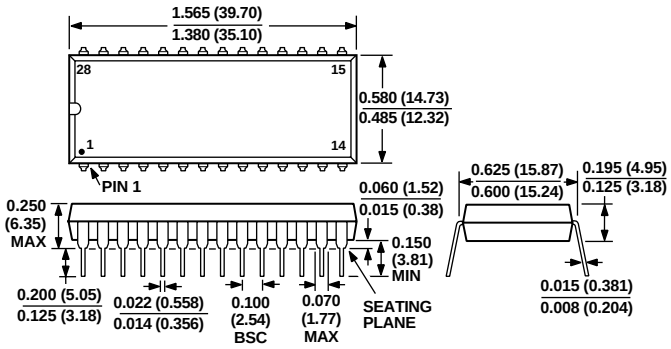
*Figure 28. Bit Clock, Word Clock, Left/$\overline{Right}$ Clock and Data Timing*

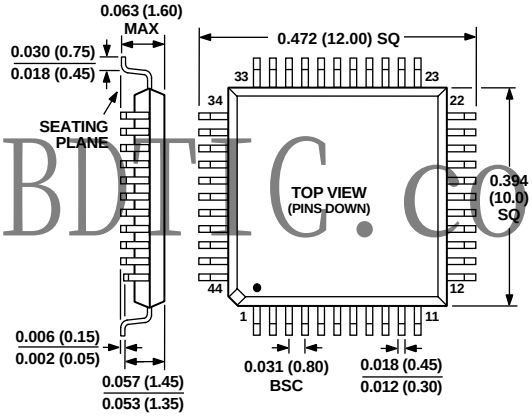
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 28-Lead Plastic DIP
### (N-28)




### 44-Lead LQFP
### (ST-44)

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